Notice of Allowability	Application No.	Applicant(s)	
	10/645,201	KIZER, JADE M.	
	Examiner	Art Unit	
	Brian D. Nguyen	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on 10/5/05*.

2. ☒ The allowed claim(s) is/are *1-3, 7-12, 6, 13-17, 19-24, 18, 25-29, 31-36, 30, 37-40, 42-51 (renumbered 1-48, respectively)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *12142005* .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

BRIAN NGUYEN
PRIMARY EXAMINER 12/14/05

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Mark Haynes on 12/14/05.

3. The application has been amended as follows:

Claim 1. A signal interface, comprising:

a set of signal lines having N+1 signal lines, where N is an integer;

N+1 receivers coupled to respective signal lines in the set of signal lines establishing a set of N+1 signal paths with the set of signal lines;

an N line bus;

a line maintenance circuit; and

a switch in the N+1 signal paths, and control logic for the switch, which selectively routes N signal paths in the set to the N line bus and signal path (n) in the set to the line maintenance circuit, where (n) is changed according to a pattern to selectively maintain signal paths in the set of N+1 signal paths while enabling data flow on N signal paths in the set to the N line bus; wherein for a change of (n) by switching a first particular signal path from routing to the line maintenance circuit to routing to a line in the N line bus, and a second particular signal path from routing to the line in the N line bus to the line maintenance circuit, the control logic controls the switch so that reception of data from the line in the N line bus is uninterrupted; and

wherein the receivers are responsive to respective receive clock signals produced by adjustable clock generators, and said line maintenance circuit sets the adjustable clock generators in response to a calibration data pattern on the signal path coupled to the line maintenance circuit.

Claim 4. (Cancelled).

Claim 5. (Cancelled).

Claim 6. A signal interface, comprising:

a set of signal lines having N+1 signal lines, where N is an integer;

N+1 receivers coupled to respective signal lines in the set of signal lines establishing a set of N+1 signal paths with the set of signal lines;

an N line bus;

a line maintenance circuit; and

a switch in the N+1 signal paths, and control logic for the switch, which selectively routes N signal paths in the set to the N line bus and signal path (n) in the set to the line maintenance circuit, where (n) is changed according to a pattern to selectively maintain signal paths in the set of N+1 signal paths while enabling data flow on N signal paths in the set to the N line bus ,wherein for a change of (n) by switching a first particular signal path from routing to the line maintenance circuit to routing to a line in the N line bus, and a second particular signal path from routing to the line in the N line bus to the line maintenance circuit, the control logic controls the switch so that during a settling interval, the first and second particular signal paths both carry data from the line in the N line bus, and then after the settling interval the second particular signal path is coupled to the line maintenance circuit; and

wherein the receivers are responsive to respective receive clock signals produced by adjustable clock generators, and said line maintenance circuit sets the adjustable clock generators in response to a calibration data pattern on the signal path coupled to the line maintenance circuit.

Claim 9. The signal interface of claim 1, further including logic to power down the N+1 receivers while continuing to selectively maintain signal paths in the set of signal paths.

Claim 13. A signal interface, comprising:

an N line bus;

a set of signal lines having N+1 signal lines, where N is an integer;

N+1 transmitters coupled to respective signal lines in the set of signal lines establishing a set of N+1 signal paths with the set of signal lines;

a line maintenance circuit; and

a switch in the N+1 signal paths, and control logic for the switch, which selectively routes N signal paths in the set from the N line bus to N signal lines in the set of signal lines, and routes signal path (n) in the set from the line maintenance circuit to signal line (n) in the set of signal lines, where (n) is changed according to a pattern to selectively perform maintenance on signal paths in the set of N+1 signal paths while enabling data flow on N signal paths in the set from the N line bus; wherein for a change of (n) by switching a first particular signal path from routing to the line maintenance circuit to routing to a line in the N line bus, and a second particular signal path from routing to the line in the N line bus to the line maintenance circuit, the control logic controls the switch so that transmission of data from the line in the N line bus is uninterrupted; wherein receivers coupled to the signal lines are responsive to respective receive

clock signals produced by corresponding adjustable clock generators, and a line maintenance circuit coupled with the receivers sets the adjustable clock generators in response to a calibration data pattern on the signal path coupled to the line maintenance circuit coupled with the receivers.

Claim 18. A signal interface, comprising:

an N line bus;

a set of signal lines having N+1 signal lines, where N is an integer;

N+1 transmitters coupled to respective signal lines in the set of signal lines establishing a set of N+1 signal paths with the set of signal lines;

a line maintenance circuit; and

a switch in the N+1 signal paths, and control logic for the switch, which selectively routes N signal paths in the set from the N line bus to N signal lines in the set of signal lines, and routes signal path (n) in the set from the line maintenance circuit to signal line (n) in the set of signal lines, where (n) is changed according to a pattern to selectively perform maintenance on signal paths in the set of N+1 signal paths while enabling data flow on N signal paths in the set from the N line bus for a change of (n) by switching a first particular signal path from routing from the line maintenance circuit to routing to a line in the N line bus, and a second particular signal path from routing to the line in the N line bus from the line maintenance circuit, the control logic controls the switch so that during a settling interval, the first and second particular signal paths both carry data to the line in the N line bus, and then after the settling interval the second particular signal path is coupled to the line maintenance circuit; and

wherein receivers coupled to the signal lines are responsive to respective receive clock signals produced by corresponding adjustable clock generators, and a line maintenance circuit

coupled with the receivers sets the adjustable clock generators in response to a calibration data pattern on the signal path coupled to the line maintenance circuit coupled with the receivers.

Claim 21. The signal interface of claim 13, further including logic to power down the N+1 transmitters while continuing to selectively perform maintenance on signal paths in the set of N+1 signal paths.

Claim 25. A communication system for inter-chip signals, comprising:

a first integrated circuit, a second integrated circuit, and a set of N+1 communications lines between the first and second integrated circuits;

the first integrated circuit comprising

a first N line bus, where N is an integer;

a set of transmitter signal lines having N+1 transmitter signal lines coupled to respective communications lines in the set of N+1 communications lines;

N+1 transmitters coupled to respective transmitter signal lines in the set of transmitter signal lines establishing a set of N+1 transmitter signal paths with the set of transmitter signal lines;

a calibration signal source; and

a switch in the N+1 transmitter signal paths, and first control logic which selectively routes N transmitter signal paths in the set from the first N line bus to N transmitter signal lines in the set of signal lines, and routes transmitter signal path (n) in the set from the calibration signal source to one transmitter signal line in the set of transmitter signal lines, where (n) is changed according to a pattern to selectively supply calibration signals on communication

lines in the set of N+1 communication lines while enabling data flow on N communication lines in the set from the first N line bus; and

the second integrated circuit comprising

a set of receiver signal lines having N+1 receiver signal lines coupled to respective communications lines in the set of N+1 communications lines;

N+1 receivers coupled to respective receiver signal lines in the set of receiver signal lines establishing a set of N+1 receiver signal paths with the set of receiver signal lines;

a second N line bus;

a calibration circuit; and

a switch in the N+1 receiver signal paths, and second control logic, which selectively routes N receiver signal paths in the set to the second N line bus and receiver signal path (n) in the set to the calibration circuit, where (n) is changed according to the pattern to selectively calibrate receiver signal paths in the set of N+1 receiver signal paths while enabling data flow on N receiver signal paths in the set to the second N line bus; and

wherein the receivers are responsive to respective receive clock signals produced by adjustable clock generators, and said line maintenance circuit sets the adjustable clock generators in response to a calibration data pattern on the signal path coupled to the calibration circuit; and

control logic on at least one of the first and second integrated circuits; wherein for a change of (n) by switching a first particular signal path from routing between the calibration signal source and the calibration circuit to routing to between lines in the first and second N line buses, and a second particular signal path from routing between lines in the first and second N line buses to routing between the calibration signal source and the calibration circuit, the control

logic controls the switch so that transmission of data from between the lines in the first and second N line buses is uninterrupted.

Claim 30. A communication system for inter-chip signals, comprising:

a first integrated circuit, a second integrated circuit, and a set of N+1 communications lines between the first and second integrated circuits;

the first integrated circuit comprising:

a first N line bus, where N is an integer;

a set of transmitter signal lines having N+1 transmitter signal lines coupled to respective communications lines in the set of N+1 communications lines;

N+1 transmitters coupled to respective transmitter signal lines in the set of transmitter signal lines establishing a set of N+1 transmitter signal paths with the set of transmitter signal lines;

a calibration signal source; and

a switch in the N+1 transmitter signal paths, and first control logic which selectively routes N transmitter signal paths in the set from the first N line bus to N transmitter signal lines in the set of signal lines, and routes transmitter signal path (n) in the set from the calibration signal source to one transmitter signal line in the set of transmitter signal lines, where (n) is changed according to a pattern to selectively supply calibration signals on communication lines in the set of N+1 communication lines while enabling data flow on N communication lines in the set from the first N line bus; and

the second integrated circuit comprising:

a set of receiver signal lines having N+1 receiver signal lines coupled to respective communications lines in the set of N+1 communications lines;

N+1 receivers coupled to respective receiver signal lines in the set of receiver signal lines establishing a set of N+1 receiver signal paths with the set of receiver signal lines;

a second N line bus;

a calibration circuit; and

a switch in the N+1 receiver signal paths, and second control logic, which selectively routes N receiver signal paths in the set to the second N line bus and receiver signal path (n) in the set to the calibration circuit, where (n) is changed according to the pattern to selectively calibrate receiver signal paths in the set of N+1 receiver signal paths while enabling data flow on N receiver signal paths in the set to the second N line bus; and

wherein the receivers are responsive to respective receive clock signals produced by adjustable clock generators, and said line maintenance circuit sets the adjustable clock generators in response to a calibration data pattern on the signal path coupled to the calibration circuit; and

wherein for a change of (n) by switching a first particular transmitter signal path from routing from the calibration signal source to routing from a line in the first N line bus, and a second particular transmitter signal path from routing from the line in the first N line bus to routing from the calibration signal source, the first control logic controls the switch in the N+1 transmitter signal paths so that during a settling interval, the first and second particular transmitter signal paths both carry data from the line in the first N line bus, and then after the settling interval the second particular signal path is routed from the calibration signal source.

Claim 31. The communication system of claim 25 [~~30~~], wherein for a change of (n) by switching a first particular receiver signal path from routing to the calibration circuit to routing to a line in the second N line bus, and a second particular receiver signal path from routing to the line in the second N line bus to the calibration circuit, the second control logic controls the switch in the N+1 receiver signal paths so that during a settling interval, the first and second particular receiver signal paths both carry data for the line in the second N line bus, and then after the settling interval the second particular receiver signal path is coupled to the calibration circuit.

Claim 37. A method for managing a high speed communication interface for a parallel bus having N bus lines, where N is an integer, comprising:

establishing N+1 communication lines;

performing a maintenance operation on communication line (n) of the N+1 communications lines and enabling paths from the N bus lines on N of the N+1 communications lines, wherein receivers on the N+1 communications lines are responsive to respective receive clock signals produced by adjustable clock generators, and said maintenance operation sets the adjustable clock generators in response to a calibration data pattern transmitted on the communication line (n);

after performing the maintenance operation on communication line (n) of the N+1 communications lines, changing (n) and performing a maintenance operation a next communication line of the N+1 communication lines; and for a changing (n) to switch a first particular communication line from subject of the maintenance operation to communicating from a line on the N line bus, and a second particular communication line from communicating from

the line on the N line bus to subject of the maintenance operation, routing the first and second particular communication lines so that both carry data from the line in the N line bus during a settling interval, and then after the settling interval performing the maintenance operation on the second particular communication line.

Claim 41. (Cancelled).

Claim 47. A signal interface, comprising:

a set of signal lines;

a set of receivers coupled to respective signal lines in the set of signal lines;

a bus comprising a set of bus lines;

a line maintenance circuit; and

a switch coupled to the set of receivers, to the bus and to the line maintenance circuit, and control logic for the switch, which selectively routes signals in parallel from receivers in the set of receivers to bus lines in the set of bus lines and to the line maintenance circuit, where the receiver in the set of receivers routed to the line maintenance circuit is changed according to a pattern to selectively maintain signal paths over said set of signal lines without interrupting data flow from the set of receivers from the set of signal lines; and

wherein the receivers are responsive to respective receive clock signals produced by adjustable clock generators, and said line maintenance circuit sets the adjustable clock generators in response to a calibration data pattern on the signal path coupled to the calibration circuit.

Claim 48. A transmission circuit on an integrated circuit, comprising:

a line maintenance circuit to output a line maintenance signal;

a set of transmitters coupled to receive a first set of signals and the line maintenance signal, and to output a second set of signals, wherein the second set of signals includes the first set of signals and the maintenance signal; and

a switch coupled to the set of transmitters and a control logic for the switch, to selectively route the first set of signals and the line maintenance signal in parallel to the set of transmitters, where the transmitter in the set of transmitters routed to the line maintenance circuit is changed according to a pattern to selectively maintain the second set of signals from the set of transmitters and to permit the maintenance signal to be used as a calibration signal, the transmitter in the set of transmitters routed to the line maintenance circuit is changed without interruption of transmission of the first set of signals, wherein receivers adapted to receive the second set of signals are responsive to respective receive clock signals produced by corresponding adjustable clock generators, and a line maintenance circuit coupled with the receivers sets the adjustable clock generators in response to a calibration data pattern in the maintenance signal.

Claim 49. A receiver circuit on an integrated circuit, comprising:

means for receiving a first set of signals and a line maintenance signal, and to output a second set of signals;

means for calibrating the means for receiving without interrupting the outputting of the second set of signals, the means for calibrating coupled to receive the line maintenance signal;

means for routing the first set of signals and the line maintenance signal in parallel from the means for receiving, wherein the routing changes according to a pattern to selectively

maintain the second set of signals and to permit the maintenance signal to be used as a maintenance signal for maintaining different portions of the means for receiving; and

wherein the maintenance signal comprises a calibration data pattern, and the means for receiving includes receivers that are responsive to respective receive clock signals produced by adjustable clock generators, and said means for calibrating sets the adjustable clock generators in response to the calibration data pattern.

Claim 50. A signal interface, comprising:

a set of signal lines having N+1 signal lines, where N is an integer;

N+1 receivers coupled to respective signal lines in the set of signal lines establishing a set of N+1 signal paths with the set of signal lines;

an N line bus;

a line maintenance circuit; and

a switch in the N+1 signal paths, and control logic for the switch, which selectively routes N signal paths in the set to the N line bus and signal path (n) in the set to the line maintenance circuit, where (n) is changed according to a pattern to selectively maintain signal paths in the set of N+1 signal paths while enabling data flow on N signal paths in the set to the N line bus; wherein the line maintenance circuit performs calibration of the receiver coupled to signal path (n) routed to the line maintenance circuit, independent of the data flow on the N line bus; and

wherein the receivers are responsive to respective receive clock signals produced by adjustable clock generators, and said line maintenance circuit sets the adjustable clock generators in response to a calibration data pattern on the signal path coupled to the calibration circuit.

Claim 51. A signal interface, comprising:

an N line bus;

a set of signal lines having N+1 signal lines, where N is an integer;

N+1 transmitters coupled to respective signal lines in the set of signal lines establishing a set of N+1 signal paths with the set of signal lines;

a line maintenance circuit; and

a switch in the N+1 signal paths, and control logic for the switch, which selectively routes N signal paths in the set from the N line bus to N signal lines in the set of signal lines, and routes signal path (n) in the set from the line maintenance circuit to signal line (n) in the set of signal lines, where (n) is changed according to a pattern to selectively perform maintenance on signal paths in the set of N+1 signal paths while enabling data flow on N signal paths in the set from the N line bus, independent of the data flow on the N line bus; wherein receivers coupled to the signal lines are responsive to respective receive clock signals produced by corresponding adjustable clock generators, and a line maintenance circuit coupled with the receivers sets the adjustable clock generators in response to a calibration data pattern on the signal path coupled to the line maintenance circuit coupled with the receivers.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian D. Nguyen whose telephone number is (571) 272-3084. The examiner can normally be reached on 7:30-6:00 Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on (571) 272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

12/14/05

BRIAN NGUYEN
PRIMARY EXAMINER